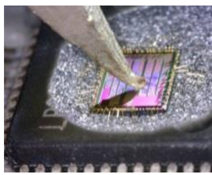

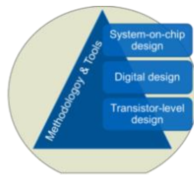

Technische Universität München

Department of Electrical and
Computer Engineering

Invitation to TUM-DECS Workshop

Security and Reliability in Electronic Circuits

Tuesday, February 24, 2015, 13:00-17:30, Room 4905

(**Maps**: https://portal.mytum.de/campus/roomfinder/search_room_results?searchstring=4905&building=0509&search=Suche+starten)

Session 1: Security

13:00 Statistic-Based Security Analysis of Ring Oscillator PU
Florian Wilde, Institute for Security in Information Technology
Abstract: Ring oscillators (ROs) are a robust way to implement a physical unclonable function (PUF) into ASICs or FPGAs, but claims of predictability arose recently. We describe why this probably results from not using adjacent ROs for pairwise comparison because of spatial patterns in mean frequency and correlations found by principal component analysis. Apart from that, we outline that devices with proximate serial numbers are not more similar than other devices.

13:20 Automated Verification of masked Netlists
Michael Tempelmeier, Institute for Security in Information Technology
Abstract: Today's synthesis tools do a fairly good job optimizing a circuit in terms of power consumption, speed or area and a lot of research is done to improve this capabilities even more. Optimizing circuits however leads to a sea of gates with no regular structure. This makes reasoning about correct masking particularly challenging. In this presentation we will present an approach to tackle this problem.

Session 2: Reliability during design

13:40 Detection of Aging Critical Structures and Conditions in Power-Down Mode
Michael Zwerger, Institute for Electronic Design Automation
Abstract: In power-down mode of analog circuit reliability problems can occur due to asymmetric stress at matched devices. In this talk, a method for automatic detection of asymmetric stress at critical structures is outlined.

14:00-14:30 Coffee&Posters

14:30 Integrating Aging Aware Timing Analysis into a Commercial STA Tool
Shushanik Karapetyan, Institute for Electronic Design Automation
Abstract: With the continuous scaling of transistor sizes, aging effects such as NBTI and HCI become more and more pronounced. Traditionally, aging analysis has not been a part of the established circuit design flow and commercial tools do not yet support aging analysis on gate level, therefore aging analysis is not commonly available to industrial designers yet. This work presents an automated methodology for fast and accurate NBTI and HCI aware timing analysis. The approach utilizes the AgeGate aging aware gate model and integrates it into a commercial static timing analysis (STA) tool (Synopsys PrimeTime). The paper presents results obtained from applying the method to various benchmark circuits. These results demonstrate that aging is relevant and that it can efficiently be analyzed using commercial tools.

14:50 Implementation of Fine-grained Approximate Sequential Circuits
David May, Institute for Integrated Systems
Abstract: Approximate Computing is a novel approach to substantially decrease the power consumption of integrated circuits. By tolerating a certain number of errors within the circuit, it can be operated at more resource-saving state. I.e. the area overhead due to redundancy can be reduced, supply-voltage can be decreased or even parts of the circuit could be even switched off. Clearly, not all applications are suitable for such an approach. And even in these applications one has to be very careful when tolerating faults. In this talk I am going to present a complete flow, from application to RTL, in order to find out where, and to what extend faults can be tolerated in a certain application.

Session 3: Reliability during operation

15:10 Matching Detection & Correction Schemes for Soft Error Handling in Sequential Logic
Erol Koser, Institute for Integrated Systems
Abstract: A huge number of soft error detection and correction schemes have been published in recent years. However if detection and correction are separated, in both domains idealized assumptions are made. In this presentation we will show a scenario were the assumptions do not match. Afterwards a modification (or mix) of standard approaches is introduce to enable an overall soft error handling scheme.

15:30-16:00 Coffee&Posters

16:00 Efficient communication reconfiguration for task migration and the dependability of manycore SoCs
Stefan Rösch, Institute for Integrated Systems
Abstract: Bit faults caused by ionizing radiation, aging effects and thermal hotspots are major challenges for the reliability of future CMOS systems. In modern MPSoCs, these impacts can be tackled at system level with proactive task relocation or redundant task execution. In both cases, the channels of the intertask communication must be adapted to the dynamic and flexible task mapping during runtime.
This talk will present a communication reconfiguration protocol for this purpose. Three different schemes for channel reconfiguration (stop & resume, packet duplication and packet forwarding) are evaluated according to their impacts on the task execution on different system configurations.

16:20 Power Efficient Digital IC Design for a Medical Application with High Reliability Requirements
Nasim Pour Aryan, Institute for Technical Electronics
Abstract: For a design which is tolerant to parameter variations caused by process, voltage, temperature and aging, precise monitoring of the reliability status becomes a prerequisite. In applications such as medical implants reliability in combination with power efficiency is a crucial design goal. In the monitoring approach presented in this work, circuit level timing properties are measured and utilized for reliability diagnosis. In situ timing monitors are inserted and fabricated within the digital front end of a neural measurement system. The monitors can distinguish between critical and relaxed operation. Extracted timing information is used for on-line adaptation of the supply voltage in order to reduce aging as well as the power consumption of the implants. The supply voltage of the digital circuitry is decreased to the minimum possible value, while ensuring reliable operation of the circuit.

16:40-17:30 Podium&Discussion&Coffee&Posters

The schedule is tentative. It will be adapted according to emerging discussion.

The workshop is presented by the Center of Competence "Design of Electronic Circuits (DECS)" of the TUM ECE department (http://www.ei.tum.de/en/research/coc-decs/) and its members: Georg Sigl (Coordinator) and Michael Pehl (SEC), Andreas Herkersdorf and Walter Stechele (LIS), Doris Schmitt-Landsiedel (LTE), Josef A. Nossek and Michel T. Ivrlac (NWS), Ulf Schlichtmann and Helmut Graeb (EDA).

The workshop is sponsored by the Institute of Electronic Design Automation (Prof. Schlichtmann) http://eda.ei.tum.de