Dr. Eishi **Arima**

Scientific Staff (Wissenschaftliche Mitarbeiter)

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Work Experience

Employment

Technical University of Munich (Technische Universität München) — *Garching, Germany*

Scientific Staff (Wissenschaftliche Mitarbeiter) — *Apr. 2021 - present*

- Informatics 10, Department of Informatics

The University of Tokyo — *Tokyo, Japan*

Project Research Associate (or Project Assistant Professor) — *Apr. 2016 - Mar. 2021*

- Supercomputing Research Division, Information Technology Center

The University of Tokyo — *Tokyo, Japan*

Research Assistant — *Apr. 2012 - Mar. 2016*

- Graduate School of Information Science and Technology

Guest Scientist

Technical University of Munich (Technische Universität München) — *Garching, Germany*

External Scientist — *Jun. 2018 - Mar. 2019*

- Informatics 10, Department of Informatics

Lawrence Livermore National Laboratory — *CA, US*

Visiting Scientist — *Oct. 2016 - Oct. 2017*

- Center for Applied Scientific Computing

RIKEN R-CCS — *Hyogo, Japan*

Visiting Scientist — *May. 2016 - Mar. 2021*

- Architecture Development Team

Education

The University of Tokyo — *Tokyo, Japan*

Ph.D in Information Science and Technology — *Mar. 2016*

- Cache Design Optimization for Energy-Efficient Processors

The University of Tokyo — *Tokyo, Japan*

Master of Information Science and Technology — *Mar. 2013*

- Power Reduction of Cache Memory in Idle State

The University of Tokyo — *Tokyo, Japan*

Bachelor of Engineering — *Mar. 2011*

- A High-Resolution Book Digitization System Based on High-Speed 3D Shape Recognition

Research Summary

My broader research interests are principally in high performance computing (HPC), computer architecture, and system software, while the recent major focuses are on (1) resource/power management in HPC systems; (2) heterogeneous system/processor/memory architectures; (3) performance/power modeling, analysis, and optimization; and (4) software/hardware interactions and interfaces. In particular, I am currently involved in REGALE project in order for investigating holistic and sophisticated power/resource management techniques for large-scale HPC systems. Further, I have conducted several microarchitecture-level hardware studies including (1) memory system design optimizations based on emerging device technologies and (2) evaluations and design space explorations for SIMD-based HPC microprocessors.

Publications and Talks

Publications

1. Urvij Saroliya, Eishi Arima, Dai Liu, Martin Schulz "Reinforcement Learning-driven Co-scheduling and Diverse Resource Assignments on NUMA Systems" In *Proceedings of The 42nd IEEE International Conference on Computer Design (**ICCD**)*, pp.170–178, Nov., 2024 (**acceptance rate: 74/277=27%**)
2. Mohak Chadha, Thandayuthapani Subramanian, Eishi Arima, Michael Gerndt, Martin Schulz, Osama Abboud "GreenCourier: Carbon-Aware Scheduling for Serverless Functions" In *Proceedings of the 9th International Workshop on Serverless Computing 2023 (WOSC9)*, pp 18-23, Dec., 2023
3. Mohak Chadha, Eishi Arima, Amir Raoofy, Michael Gerndt, Martin Schulz "Sustainability in HPC: Vision and Opportunities" In *Proceedings of Sustainable Supercomputing*, pp.1876-1880, Nov., 2023
4. Urvij Saroliya, Eishi Arima, Dai Liu, Martin Schulz "Hierarchical Resource Partitioning on Modern GPUs: A Reinforcement Learning Approach" In *Proceedings of IEEE International Conference on Cluster Computing (**CLUSTER**)*, pp.185-196, Nov., 2023 (**acceptance rate: 31/130=24%**)
5. Isaías A. Comprés, Eishi Arima, Martin Schulz, Tiberiu Rotaru, and Rui Machado "Probabilistic Job History Conversion and Performance Model Generation for Malleable Scheduling Simulations" In *Proceedings of ISC High Performance Workshops*, pp.82-94, May, 2023
6. Issa Saba, Eishi Arima, Dai Liu, Martin Schulz "Orchestrated Co-Scheduling, Resource Partitioning, and Power Capping on CPU-GPU Heterogeneous Systems via Machine Learning", In *Proceedings of 35th GI/ITG International Conference on Architecture of Computing Systems (ARCS)*, pp.51-67, Sep., 2022
7. Eishi Arima, Minjoon Kang, Issa Saba, Josef Weidendorfer, Carsten Trinitis, Martin Schulz "Optimizing Hardware Resource Partitioning and Job Allocations on Modern GPUs under Power Caps", In *Proceedings of International Conference on Parallel Processing Workshops*, no. 9, pp.1-10, Aug., 2022
8. Eishi Arima, Isaías A Comprés, Martin Schulz "On the Convergence of Malleability and the HPC PowerStack: Exploiting Dynamism in Over-Provisioned and Power-Constrained HPC Systems", In *Proceedings of ISC High Performance Workshops*, pp.206-217, Jun., 2022
9. Eishi Arima, Yuetsu Kodama, Tetsuya Odajima, Miwako Tsuji, Mitsuhisa Sato, "Power/Performance/Area Evaluations for Next-Generation HPC Processors using the A64FX Chip", In *Proceedings of IEEE Symposium on Low-Power and High-Speed Chips and Systems*, 6pages, Apr., 2021
10. Yuetsu Kodama, Tetsuya Odajima, Eishi Arima, Mitsuhisa Sato, "Evaluation of Power Management Control on the Supercomputer Fugaku", In *Proceedings of 2020 IEEE International Conference on Cluster Computing (CLUSTER)*, EEHPC volume, pp. 484-493, Sep., 2020
11. Eishi Arima, "Classification-Based Unified Cache Replacement via Partitioned Victim Address History", In *Proceedings of 2020 23rd Euromicro Conference on Digital System Design (DSD)*, pp.101-108, Aug., 2020
12. Eishi Arima, Toshihiro Hanawa, Carsten Trinitis, Martin Schulz, "Footprint-Aware Power Capping for Hybrid Memory Based Systems", In *Proceedings of the 35th International Conference on High Performance Computing, ISC High Performance 2020 (**ISC**)*, pp.347-369, Jun., 2020 (**acceptance rate: 27/87=31%**)
13. Eishi Arima, Martin Schulz, "Pattern-Aware Staging for Hybrid Memory Systems", In *Proceedings of the 35th International Conference on High Performance Computing, ISC High Performance 2020 (**ISC**)*, pp.474-495, Jun., 2020 (**acceptance rate: 27/87=31%**)
14. Hiroki Noguchi, Kazutaka Ikegami, Satoshi Takaya, Eishi Arima, Atsushi Kawasumi, Hiroyuki Hara, Keiko Abe, Naoharu Shimomura, Junichi Ito, Shinobu Fujita, Takashi Nakada, Hiroshi Nakamura, "4Mb STT-MRAM-based Cache with Memory-Access-aware Power Optimization and Novel Write-Verified-Write / Read-Modified-Write Scheme", In *Proceedings of 2016 IEEE International Solid-State Circuits Conference (**ISSCC**)*, pp.132–133, Feb., 2016 (**acceptance rate: 200/595=34%**)
15. Susumu Takeda, Hiroki Noguchi, Kumiko Nomura, Shinobu Fujita, Shinobu Miwa, Eishi Arima, Takashi Nakada, Hiroshi Nakamura, "Low-power cache memory with state-of-the-art STT-MRAM for high-performance processors", In *Proceedings of the 12th International SoC Design Conference (ISOCC)*, pp.153–154, Nov., 2015
16. Eishi Arima, Hiroki Noguchi, Takashi Nakada, Shinobu Miwa, Susumu Takeda, Shinobu Fujita, Hiroshi Nakamura, "Immediate Sleep: Reducing Energy Impact of Peripheral Circuits in STT-MRAM Caches", In *Proceedings of the 33rd IEEE International Conference on Computer Design (**ICCD**)*, pp.149–156, Oct. 2015 (**acceptance rate: 83/269=31%**)
17. Eishi Arima, Toshiya Komoda, Takashi Nakada, Shinobu Miwa, Hiroki Noguchi, Kumiko Nomura, Keiko Abe, Shinobu Fujita, Hiroshi Nakamura, "Analyzing Requirements Specification of STT-MRAM Last Level Cache Considering Low CPU Loads", *IEICE Transactions*, Vol.J97-A, No.10, pp.629-647, 2014 (in Japanese)
18. Eishi Arima, Toshiya Komda, Takashi Nakada, Shinobu Miwa, Hiroshi Nakamura, "Lost Data Prefetching to Reduce Performance Degradation Caused by Powering off Caches", *IPSJ Transaction of Advanced Computing Systems*, Vol.6, No.3, pp.118-130, 2013 (in Japanese)
19. Hiroki Noguchi, Kumiko Nomura, Keiko Abe, Shinobu Fujita, Eishi Arima, Kyundong Kim, Takashi Nakada, Shinobu Miwa, Hiroshi Nakamura, "D-MRAM Cache: Enhancing Energy Efficiency with 3T-1MTJ DRAM/MRAM Hybrid Memory", In *Proceedings of Design, Automation & Test in Europe Conference & Exhibition (**DATE**)*, pp.1813–1818, Mar., 2013 (**acceptance rate: 206/829=25%**)

Conference Posters or Workshop Presentations (Refereed)

20. Eishi Arima, Carsten Trinitis, Martin Schulz "Toward Dynamic Orchestration of Data/Power/Process Management for Hybrid Memory Based Systems", In *Tagungsband des FG-BS Herbsttreffens*, 3pages, Sep., 2021
21. Eishi Arima, Carsten Trinitis, "A Case for Co-Scheduling for Hybrid Memory Based Systems", *48th International Conference on Parallel Processing (ICPP)*, Poster Session, Aug., 2019
22. Eishi Arima, Toshihiro Hanawa, Martin Schulz, "Toward Footprint-Aware Power Shifting for Hybrid Memory Based Systems", *47th International Conference on Parallel Processing (ICPP)*, Poster Session, Aug., 2018
23. Eishi Arima, Hiroshi Nakamura, "Page Table Walk Aware Cache Management for Efficient Big Data Processing", *Big Data Benchmarks, Performance Optimization, and Emerging Hardware (BPOE-8) (in conjunction with 22nd ACM International Conference on Architectural Support for Programming Languages and Operating Systems)*, Apr., 2017
24. Eishi Arima, Hiroki Noguchi, Takashi Nakada, Shinobu Miwa, Susumu Takeda, Shinobu Fujita, Hiroshi Nakamura, "Subarray Level Power-Gating in STT-MRAM Caches to Mitigate Energy Impact of Peripheral Circuits", *52nd ACM/EDAC/IEEE Design Automation Conference (DAC)*, Work-in-Progress Session, June, 2015
25. Eishi Arima, Hiroki Noguchi, Takashi Nakada, Shinobu Miwa, Susumu Takeda, Shinobu Fujita, Hiroshi Nakamura, "Fine-Grain Power-Gating on STT-MRAM Peripheral Circuits with Locality-aware Access Control", *The Memory Forum (in conjunction with the 41st International Symposium on Computer Architecture)*, June, 2014

Editorship

26. Maurizio Palesi, Gianluca Palermo, Catherine Graves, Eishi Arima, "Proceedings of the 17th ACM International Conference on Computing Frontiers", CF 2020, Catania, Sicily, Italy, May 11-13, 2020. ACM 2020, ISBN 978-1-4503-7956-4

Invited Talks

27. Eishi Arima "REGALE: An open architecture to equip next generation HPC applications with exascale capabilities", E4 booth at ISC'23, May, 2023
28. Eishi Arima, Daniele Cesarini, "REGALE: From an Open Architecture to Software Integrations to Realize Holistic Power Management on Supercomputers in the Exascale Era" EESC at HiPEAC'23, Jan., 2023
29. Speaker at "BoF: Community-Driven Efforts for Energy Efficiency in HPC Software Stack", SC'22, Nov., 2022
30. Eishi Arima, "REGALE: An open architecture to equip next generation HPC applications with exascale capabilities –Technical Overview", HPC PowerStack Seminar, Nov., 2022
31. Eishi Arima, "REGALE: Holistic and Feedback-driven Resource Management for Efficient Application Execution at Exascale", HeLP-DC at HiPEAC'22, Jun., 2022
32. Eishi Arima, "REGALE: An open architecture to equip next generation HPC applications with exascale capabilities", E4 booth at ISC'22, Jun., 2022
33. Panelist at "BoF: Community-Driven Efforts for Energy Efficiency in HPC Software Stack", SC'21, Nov., 2021
34. Eishi Arima, "Ongoing Efforts on Co-scheduling and Holistic Power Management", Adaptive Resource Management for HPC Systems (Dagstuhl Seminar 21441), Nov., 2021
35. Eishi Arima, "HW/SW Optimizations for Emerging Systems: Memory Perspective", LBNL - U. Tokyo Meeting, Sep. 2019
36. Eishi Arima, "Optimizations for Computing Systems with Emerging Memory Technologies", The Asia Pacific Society for Computing and Information Technology (APSCIT), Jul. 2019
37. Eishi Arima, "Efficient Big Data Processing through Page Table Walk Aware Cache Management", ASE Seminar, Apr. 2017
38. Eishi Arima, "Revisiting Memory Systems for Energy-Efficient Supercomputers", LLNL CASC Seminar, Oct. 2016

Organized Sessions in International Conferences

39. Birds of a Feather: "The HPC PowerStack: A Community-Driven Collaboration Toward Power-Aware, Energy-Efficient, and Sustainable HPC in the Exascale Era" in ISC High Performance 2023 (**acceptance rate: 33/73=45%**)
40. Special Session#1: "ARM SVE for HPC" in CF 2021 (as a special session co-chair)
41. Special Session#2: "FPGA for HPC" in CF 2021 (as a special session co-chair)
42. + several session chair experiences (e.g., at ICPP'19, Cluster'19, ARCS'22, SC'23, etc.)

Student Mentoring

2024	**Bachelor Thesis**, Lehner, Julius “Exploring Approximate Computing in FFTs”	*TUM, Germany*
2024	**Bachelor Thesis**, Okano, Taiki “Optimizing Job Mapping on CPU-GPU-FPGA Heterogeneous Platforms via Predictive Modeling”	*TUM, Germany*
2024	**Master’s Thesis**, Saroliya, Urvij “Reinforcement Learning based Resource Management for HPC Systems”	*TUM, Germany*
2024	**Bachelor Thesis**, Senkan, Tamer Yagiz “Analyzing and Modeling the Impact of Malleability in Power-constrained HPC”	*TUM, Germany*
2024	**Master’s Thesis**, Joshi, Nandini “A Case for Shared TLB Partitioning on Modern Processors”	*TUM, Germany*
2024	**Master’s Thesis**, Pandit, Sonja “Exploring an Asymmetric CPU for Energy Efficient HPC”	*TUM, Germany*
2023	**Bachelor Thesis**, Khadem-Al-Charieh, Mohammad-Mahdi “Exploring Performance Variation-aware Job Scheduling for Sustainable HPC”	*TUM, Germany*
2023	**Bachelor Thesis**, Sutanto, James “Ranking Nodes by Energy Efficiency Using sys-sage”	*TUM, Germany*
2023	**Master’s Thesis**, Sidi Baba, Mohamed Abderrahmane “Exploring the Benefits of Co-Scheduling and Power Capping for Moldable/Malleable Jobs”	*TUM, Germany*
2023	**Bachelor Thesis**, Ketata, Mohamed Aziz “Sophisticated Job Co-scheduling and Power Management Based on Memory Footprint Predictions”	*TUM, Germany*
2023	**Bachelor Thesis**, Lieber, Heiko “Cooptimization of Job Concurrency and Power Budgeting”	*TUM, Germany*
2023	**Bachelor Thesis**, Twayana, Ayash “Exploring CMS-based hardware event counting”	*TUM, Germany*
2023	**Guided Research**, Saroliya, Urvij “Reinforcement Learning based Optimization of Co-scheduling, Resource Paritioning and Power Capping on Heterogeneous HPC Systems”	*TUM, Germany*
2023	**Master’s Thesis**, Wang, Ke “Reverse Engineering Hardware Prefetching Mechanisms for Use in sys-sage”	*TUM, Germany*
2022	**Master’s Thesis**, Faith, Rifqi Al “Optimizing Memory Capacity/Bandwidth Priorities on Modern CPU via Machine Learning”	*TUM, Germany*
2022	**Master’s Thesis**, Stobbe, Adrian “Dealing with Resource Limits for a HPC Jobs in a Distributed System”	*TUM, Germany*
2022	**Master’s Thesis**, Saba, Issa “Job Co-location and Power Budgeting for Heterogeneous HPC Systems”	*TUM, Germany*
2022	**Master’s Thesis**, Terkin, Tuana “Memory-footprint aware co-scheduling for HPC clusters”	*TUM, Germany*
2022	**Guided Research**, Krisko, Milan “Probabilistic Hardware Performance Counters”	*TUM, Germany*
2022	**Bachelor’s Thesis**, Kang, Minjoon “Co-scheduling for Modern GPUs under Power Caps”	*TUM, Germany*
2022	**Bachelor’s Thesis**, Balakirev, Aleksandr “Exploring the Benefits of Non-volatile Memory in HPC Applications” (Led by Dr. Josef Weidendorfer)	*TUM, Germany*

Grants & Awards

FY2020-FY2021	**PI**, “Coscheduling Methods for Next-Generation Large-Scaled Systems with Heterogeneous Memories”, JSPS Grant-in-Aid for Early-Career Scientist, No.20K19766, 4.29M JPY (**acceptance rate: 7496/18708=40.1%**)	*JSPS, Japan*
FY2018-FY2020	**PI**, “Exploiting High-Bandwidth and Large-Capacity on Hybrid Main Memories through Pattern-Aware Optimization”, JSPS Grant-in-Aid for Early-Career Scientist, No.18K18021, 4.16M JPY (**acceptance rate: 6256/20369=30.7%**)	*JSPS, Japan*
FY2016-FY2017	**PI**, “Memory System Optimzation for Energy Efficient Big Data Processing”, JSPS Grant-in-Aid for Research Activity Start-up, No.16H06677, 2.99M JPY (**acceptance rate: 925/3699=25.0%**)	*JSPS, Japan*

Academic Services

Organizing Committee: ACM **CF’23** (Publicity Co-Chair); HPCAsia’22 (Architecture Track Co-Chair); ACM **CF’21** (Special Session Co-Chair); ACM **CF’20** (**Program Co-Chair**); IEEE **CLUSTER’19** (Publications Chair); IEEE NVMSA’18 (Web Chair)

Program Committee: ACM/IEEE **SC’25** Research/ACM SRC Posters; AsHES@IPDPS’25; IEEE NVMSA’24; AsHES@IPDPS’24; ACM/IEEE **SC’23** Exhibitor Forum; AsHES@IPDPS’23; IEEE **HiPC’22**; CANDAR’22; xSIG’22 (JP domestic); IEEE NVMSA’22; ACM **CF’22**; IEEE **IPDPS’22**; CANDAR’21; IEEE NVMSA’21; **ISC’21** PhD Forum; xSIG’21 (JP domestic); IEEE **IPDPS’21** (system software track); IEEE **IPDPS’21** (programming model track); HPCAsia’21; IEEE **HiPC’20**; IA^3@SC’20; CANDAR’20; IEEE **Cluster’20** (posters); **ISC’20** PhD Forum; xSIG’20 (JP domestic); CANDAR’19; **ISC’19** PhD Forum; xSIG’19 (JP domestic); CANDAR’18; **ICPP’18**; IEEE NVMSA’18; SCAsia’18; HPCAsia’18; CANDAR’17; IEEE NVMSA’17

Steering Committee: HPC PowerStack (2021-); IEICE CPSY (Assistant Secretary, 2019-2021); IPSJ SIGARC (2016-2020)

Journal Reviews: IEEE TPDS (2024); Journal of Parallel and Distributed Computing (2021); Concurrency and Computation: Practice and Experience, Wiley (2021,2025); The Journal of Supercomputing, Springer (2020-); Elsevier Integration, the VLSI Journal (2019); IPSJ Transactions on Advanced Computer Systems (2017-); IEICE Transactions on Information and Systems (2016-)

Conference External Reviews: Euro-Par'23; ICCS'23; IEEE IPDPS'19

Project Proposal Review: NRDI (Hungary)